RECONFIGURABLE TRANSMISSION LINE MODEL FOR ANALOG POWER FLOW COMPUTATION

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Abstract – Accurate analog models of power system components are required in order to realize an analog computation engine for power systems. Analog computation is an area of continued interest. Among the advantages over traditional digital methods are physically realizable solutions and faster computation times. This paper focuses on the design, simulation, and hardware verification of a static transmission line model for analog power flow computation. Operational transconductance amplifiers are a key component in the model based on a previously proposed DC emulation technique of power flow computation, we exhibit reconfigurability of transmission line parameters via transconductance gain. A prototype for a three bus power system was developed and tested.

Keywords: Transmission Line Model, Analog Computation, Power Flow, Power System Emulation

1 INTRODUCTION

Analog computation of power systems is a continuing field of research[1-3]. Among the advantages over traditional digital methods are physically realizable solutions and faster computation times. In order to consummate this analog method as a viable tool in power system analysis accurate models of power system components are required. This paper presents a reconfigurable transmission line model for a specific analog computation method.

Currently power flow computation for large power systems is time intensive. The calculations are nonlinear in nature and lengthy iteration schemes are the currently preferred solution. This presents a problem as many assumptions and simplifications are required to solve the equations in a timely manner. In addition, expansion of the power grid, increasing necessity and complexity of contingency studies and introduction of economic analysis are demanding further computational burden. Traditional digital methods are too slow to solve the aforementioned demands quickly. This affects the security, reliability and market operation of power systems. Ideally a real-time computation tool is preferable, specifically in market activities and operation. Analog computation provides a viable alternative to traditional approaches.

Analog power flow computation has certain advantages over digital computation. Traditional digital methods are expensive and slow in comparison to analog computers. The power flow solution is obtained almost instantaneously regardless of the number of components in the network with analog circuits. Essentially computation time is independent of network size. Effectively the solution is obtained as quickly as the system stabilizes. Experimentation has shown the ability to calculate solutions even faster than real time. In prior research simulation time for a two machine system were typically 10^4 times shorter than the real time simulated phenomena [4]. This is following the approach of modeling generator dynamics for the purpose of transient stability evaluation. There are also barriers in the field of analog computation.

The modeling and design of analog components is one obstacle that must be overcome to take advantage of these favorable attributes analog computation exhibits. The solutions will only be as accurate as the models and measurements will allow. Without clearly defined valid models for power system components this computational method will never be realized. In addition, these models also must cater towards computational speed. Specifically in power system operation multiple runs and contingencies are required to be executed extremely quickly. A priority for these analog models is to yield valid solutions while allowing fast reconfigurability. These problems have been addressed in the design of the transmission line model presented in this paper. The model was designed for a previously proposed DC emulation technique of power flow[1] computation which is reviewed in this paper followed by the proposed line model design and validation through software simulation and hardware testing. Finally the application of this model was verified through construction and computation of power flow with a three bus power system prototype.

2 PROBLEM FORMULATION

The objective was to design a transmission line model for analog power flow computation. More specifically a steady state model for a previously proposed DC emulation power flow technique. This technique, which is quickly reviewed in this paper, indicates the nature of the line models but does not provide an actual analog hardware based model for the application. This paper proposes a versatile hardware transmission line model to realize the aforementioned DC emulation technique. To take advantage of the strengths of analog computation the hardware model should have certain characteristics such as remote high speed reconfigurability, high accuracy, low-cost and VLSI capability.

Previously analog computers were large, bulky, and had to be reconfigured by hand. VLSI technology and remote reconfigurability are necessary to alleviate these downfalls and realize fast execution of multiple calculations and contingencies. In addition, accuracy and cost of analog methods are not traditionally favorable compared to digital methods. These issues also need to be addressed for analog computation to become a viable alternative to digital computation. A robust analog transmission line model should address all of the above issues.

3 ANALOG POWER FLOW METHOD

A DC emulation power flow method has been proposed in [1] and is reviewed here for an understanding of the application of the line model in this paper. This approach utilizes multiple DC networks as shown for a three bus system in Figure 1. The system is broken up into three main components: generators, transmission lines, and loads. The generators are shown as DC voltage sources. This form of DC emulation is possible due to the fact that the emulation is executed in rectangular coordinates. The generators excite the network with real $\left(\mathrm{Re}\{E_g\}\right)$ and imaginary $\left(\mathrm{Im}\{E_g\}\right)$ voltage components and the states (voltages and currents) of these networks provide the steady-state power flow solution. The transmission line components in this emulation scheme are purely resistive. R_{Re} and R_{Im} indicate real and imaginary resistor components respectively. The subscript details which buses the lines connect.

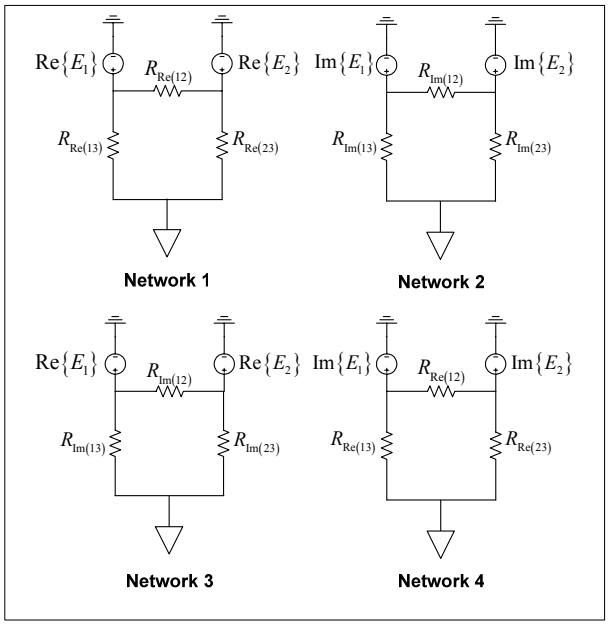

Figure 1: DC Network Emulation for a Three-Bus Power System

In addition, the imaginary resistor values are dependant upon operating frequency of the power system. By modeling these as fixed resistors the frequency is assumed to be constant For this DC emulation approach the current flowing out of a given generator i is calculated using the following equation [2]:

$$\begin{aligned} I_{Gi} &= \sum_{j=1}^{n} \mathrm{Re}\{Y_{ij}\}\cdot\mathrm{Re}\{E_j\} \quad \text{network 1} \\ &-\sum_{j=1}^{n} \mathrm{Im}\{Y_{ij}\}\cdot\mathrm{Im}\{E_j\} \quad \text{network 2} \\ &+j\sum_{j=1}^{n} \mathrm{Im}\{Y_{ij}\}\cdot\mathrm{Re}\{E_j\} \quad \text{network 3} \\ &+j\sum_{j=1}^{n} \mathrm{Re}\{Y_{ij}\}\cdot\mathrm{Im}\{E_j\} \quad \text{network 4} \end{aligned} \tag{1}$$

where $\mathrm{Re}\{E_j\}$ and $\mathrm{Im}\{E_j\}$ are the real and imaginary voltages at bus j and $\mathrm{Re}\{Y_{ij}\}$ and $\mathrm{Im}\{Y_{ij}\}$ are the real and imaginary admittances between buses i and j.

This approach accurately models and calculates power flow for a lossy transmission network with the assumption that there is no frequency deviation from nominal. A lossy transmission line model is emulated composed of both reactive and resistive elements as shown in Figure 2.

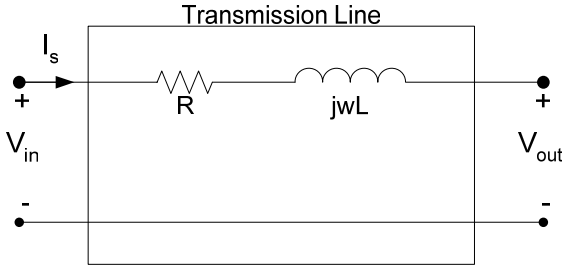

Figure 2: Lossy Transmission Line Model

Relating the emulation circuit to the real world power system determines the real and imaginary resistor values in the DC networks. The following governs this [3]:

$$R_{\mathrm{Re}(ij)} = \frac{1}{\mathrm{Re}\{Y_{ij}\}} = \frac{R_{ij}^2 + X_{Lij}^2}{R_{ij}} \tag{2}$$

$$R_{\mathrm{Im}(ij)} = \frac{1}{\mathrm{Im}\{Y_{ij}\}} = \frac{R_{ij}^2 + X_{Lij}^2}{X_{Lij}} \tag{3}$$

where R_{ij} and X_{ij} are the resistance and reactance of a line between buses i and j

The same approach is used for lossless transmission lines. The transmission line resistances are neglected as shown in Figure 3. The topology is similar to Figure 1 with the exclusion of networks 1 and 4. Similarly it is solved by (1) omitting the excluded networks.

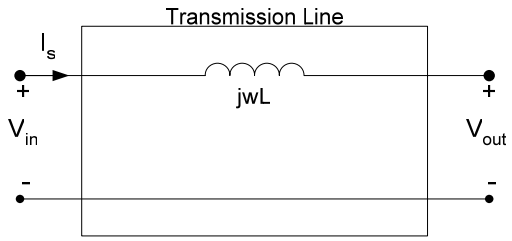

Figure 3: Lossless Transmission Line Model

The general layout for the DC emulation approach has been provided along with a relationship between AC lumped line models and the DC networks. With this information an operational transconductance amplifier (OTA) based transmission line model with reconfigurability was developed. This model was designed explicitly for the DC emulation power flow method.

4 TRANSMISSION LINE MODEL

The transmission lines were modeled as resistors in the DC emulation shown previously for both lossy and lossless lines. Actual use of resistors would require manual intervention to configure and alter the analog system. In order to overcome this problem a remotely reconfigurable OTA based variable resistor was developed to model the lines and is presented here. This device met many of the aforementioned design concerns such as remote reconfigurability.

The transconductance gain (g_m) of an OTA is controllable through an external source over a wide range, allowing remote reconfigurability. In addition, the basic OTA only consists of a few current mirrors resulting in a small and relatively low-cost device. They are also readily used in VLSI design. Due to its versatility the OTA is one of the most important building blocks of analog VLSI circuits [5] and can be highly accurate if used properly. Some of the pitfalls of OTAs are there sensitivity to temperature and saturation effects but there are methods to correct these [6, 7].

The OTA open-loop input voltage range is typically small (± 25mV) before saturation effects become extreme. This can be overcome through proper use of feedback similarly used in traditional op-amps. A CMOS design using a 2-MOSFET linear transresistor in a feedback loop has shown excellent linearity over a wide input voltage range [6]. Another complication is that the OTA gain is inversely proportional to absolute temperature. This needs to be compensated for to achieve high accuracy in large VLSI based systems where temperature differences are expected. A method is shown in [7] which alters the gain (bias current) of the OTA in direct proportion to the absolute temperature. Experimental results indicate a reduction of temperature sensitivity of more than 100 times [7].

The principle operation of an OTA is a voltage controlled current source (VCCS). Figure 4 shows an ideal OTA.

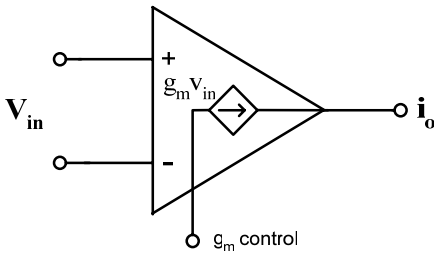

Figure 4: Ideal OTA

The amplifier has a differential voltage input and a current output. The current output is related to the differential input through a transconductance gain (g_m) controllable through an external source. Ideally the output would be:

$$i_o = g_m v_{in} \tag{4}$$

where v_{in} is the differential input voltage

With VCCS operation the OTA naturally lends itself to an application of a variable resistor. Using a single OTA in open loop operation would be the simplest implementation although it is not sufficient for this application. Current can only flow in one direction and linearity of the device is lost as the input voltage exceeds 25 mV. In the DC emulation networks the current can flow in either direction through the lines and a limitation of ± 25mV at the input would be burdensome in system configuration and measurement.

The proposed OTA based variable resistor is shown in Figure 5 [8]. It consists of two OTAs to address bi-directional current flow. When current is flowing from left to right the OTA on the right is supplying current while the OTA on the left is sinking current. The converse is true if current is flowing in the opposite direction. The inputs are floating with respect to the power supply and feedback is incorporated to extend the linear operating range of the device.

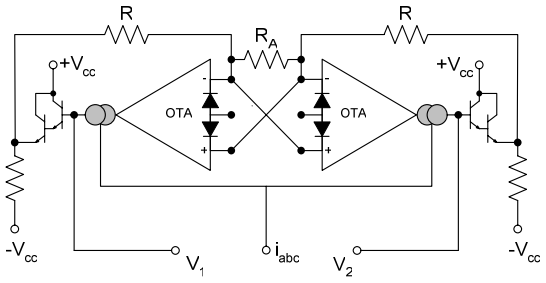

Figure 5: Double Ended OTA Transmission Line Model

This line model has three terminals similar to a variable resistor. The two inputs (V_1, V_2) mimic terminals of a resistor and the i_{abc} is the biasing current used to control the resistance of the model similar to the wiper on a potentiometer. The terminal relationship to a potentiometer is shown in Figure 6.

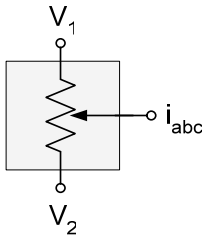

Figure 6: Potentiometer Relationship to OTA Model

The effective resistance, R_{eff}, of the OTA model is defined as the resistance seen between terminals V_1 and V_2. R_{eff} is governed directly by ohms law through the line voltage (V_{line}) and the line current (I_{line}).

$$R_{eff} = \frac{|V_1 - V_2|}{I} = \frac{V_{line}}{I_{line}} \tag{5}$$

This effective resistance is controlled by the bias current and governed by the following equation:

$$R_{eff} = \frac{2 \cdot R + R_A}{g_m \cdot R_A} \tag{6}$$

The sizing of resistors R and R_A along with the range of transconductance gain will determine the behavior of the circuit. With appropriate resistors and wide control over gain a very large range of effective resistance is obtainable. The limitations of the circuit are related to properties of OTAs. The limitations, operation and controllability were analyzed through PSPice simulations and hardware testing.

5 RESULTS

5.1 Simulation

A LM13700 dual OTA was used for the simulations in PSpice. Various simulations were run to validate and characterize the line model. Controllability, resistance variance and circuit limitations were analyzed.

The first simulation dealt with controlling the circuit through the bias current. Applying a current source is not as simple and easily controllable in comparison to a voltage source. The simulation using the circuit in Figure 7 uses a voltage source (V_{abc}) behind impedance (R_{abc}) to drive the bias current.

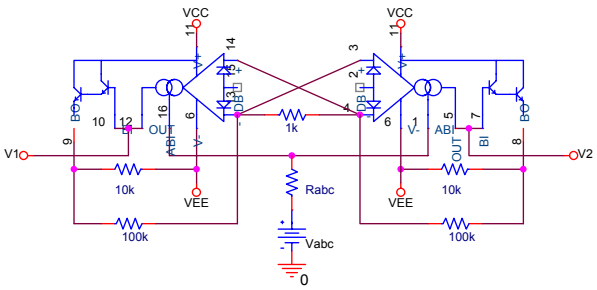

Figure 7: PSpice Schematic for Bias Current Control

A voltage sweep was performed on V_{abc} and the corresponding bias current produced was measured. The relationship between bias voltage and i_{abc} is differentiable until i_{abc} approached zero as shown in Figure 8.

From these results the following relationship between V_{abc}, R_{abc} and i_{abc} was formed:

$$i_{abc} = \frac{1}{2} \cdot \left(\frac{V_{abc} + 13.56}{R_{abc}} \right) \tag{7}$$

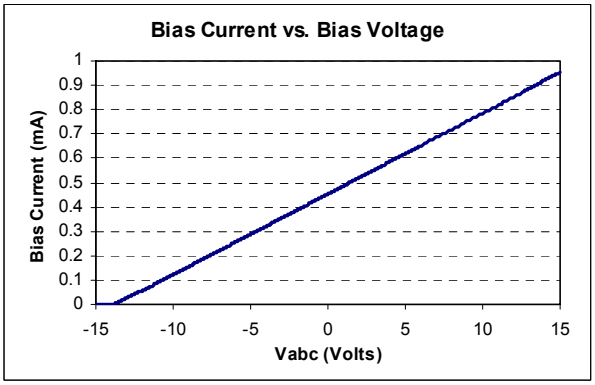

Figure 8: Bias Current vs. Bias Voltage

This approximation is close to the simulation results deviating only as the bias current becomes very close to zero. This is due to a non-linear roll-off of the bias current when compared to the bias voltage applied. Reasonable accuracy is obtained from a ± 10 Volt bias voltage.

The transconductance gain of a basic bipolar OTA is directly proportional to the bias current and is quantified by [9]:

$$g_m = \frac{i_{abc}}{2 \cdot V_T} \cdot \sec h^2 \left(\frac{V_{in}}{2 \cdot V_T} \right) \tag{8}$$

The gain in (8) is not linear, typical applications linearize g_m around an operating point. The differential input of the OTA is limited within very small range to ensure accuracy of this linear approximation. The LM13700 OTA gain is also a hyperbolic function although it improves the linearity through the use of linearizing diodes. These diodes allow a larger swing of input voltage while maintaining linear behavior. The gain for this chip, factoring in the diodes, is approximated by (9) for a differential input voltage in the range of ±50 mV. This gain can directly control the effective resistance in (6).

$$g_m \approx \frac{i_{abc}}{2 \cdot V_T} \cdot \sec h^2 \left(\frac{V_{in} \cdot D}{2 \cdot V_T} \right) \tag{9}$$

where $V_T = 26mV$ and D is a diode linearization constant

A simulation was conducted where V_{abc} was varied to change the effective resistance while holding the line

voltage constant. Figure 9 shows simulation and theoretical results from (6). The effective resistance was computed using (5). These results show the controllability of resistance over a wide range.

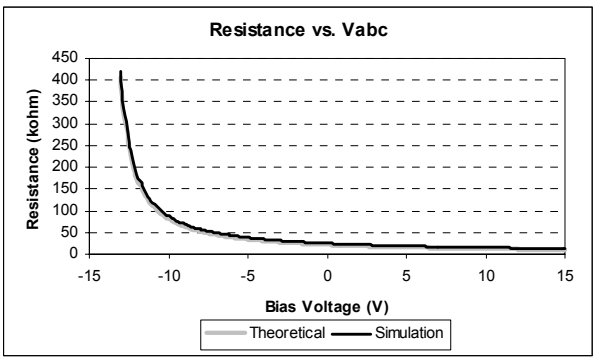

Figure 9: Theoretical and Simulated Resistance vs. Bias Voltage

More simulations were run to analyze the consistency of the resistance. While maintaining a constant bias current the circuit was subjected to varying line voltages. Figure 10 shows multiple sweeps of the line voltage with different bias currents. The plot shows line current vs. line voltage. For an ideal resistor the slope of the resulting line should be constant.

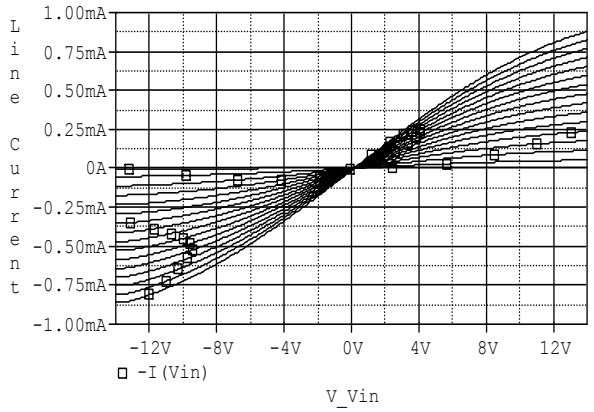

Figure 10: Line Current vs. Line Voltage

As seen from the above plot when the line voltage is between ± 4 volts the slope, or resistance, remains constant. Beyond that threshold the OTA begins to saturate. Figure 11 shows the same plot zoomed in on the linear range.

The saturation of the circuit is dependant on two factors, the bias current and the throughput current. The effective resistance has a variance of ±1% with throughput current 30% or less of the bias current. Complete saturation occurs when the throughput current is equal to the bias current. Further examination of Figure 11 reveals an offset in the circuit behavior. The output of the circuit is nonzero when no voltage is applied to the input (line terminals). This is problematic as the effective resistance of the circuit governed by ohms law is nonlinear. The computation of this resistance is shown in Figure 12 and exhibits anomalous behavior.

The offset current present at the output of the OTA is almost entirely caused by the internal offset voltage of the OTA. This can be modeled in a similar manner as offset voltages of traditional op-amps. Specifically a voltage source (v_{off}) at the input of the device is amplified to the output producing the offset (i_{offset}). For an OTA this is quantified by (10).

$$i_{offset} = v_{off} \cdot \sec h^2\left(\frac{v_{in}}{2 \cdot V_T}\right) \qquad (10)$$

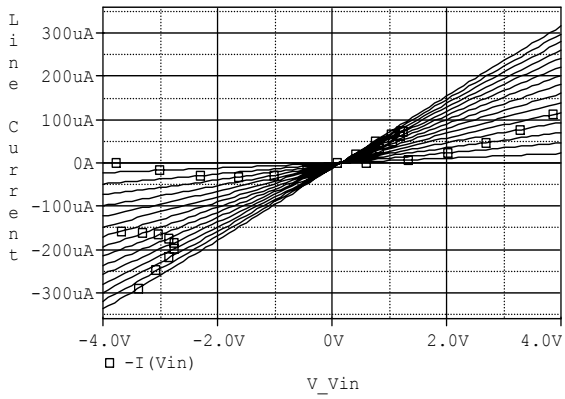

Figure 11: Line Current vs. Line Voltage Linear Region

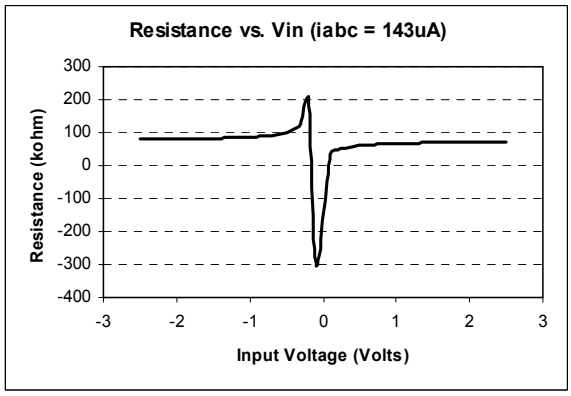

Figure 12: Effective Resistance of Line Model

A compensator could be constructed to eliminate the effects of this offset although it is more accurate to incorporate this into the fabrication. This problem is identical to the one present with traditional op-amps but the popular method of compensation, an external trimming resistor, is not sufficient for this OTA based circuit. This solution is not sufficient with reconfigurability. The effects of this offset voltage are proportional to the gain of the OTA and changes as the line model parameters are changed. Trimming can only accomplish precise offset cancellation for a single gain setting. A different approach is required.

A method for eliminating an OTA input offset voltage has been proposed in [10]. This method is suitable for fabrication and quantifies and eliminates the offset for any gain configuration. An offset rejection of 40dB was achieved in simulation [10]. With the recognition of sufficient offset cancellation the data was corrected

in a manner representing the elimination of the offset quantified by (10) to analyze the results with offset compensation. The corresponding results are much better. Figure 13 shows effective resistance versus line voltage for various bias current setting corrected for the offset. The asymptotic behavior is eliminated and the resistance exhibits a variance of approximately 1% with a line voltage magnitude of 2.5 volts or less.

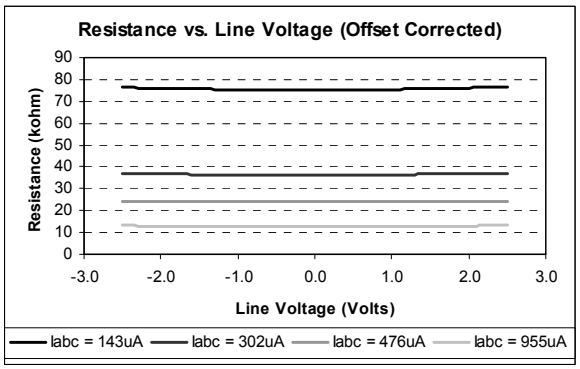

Figure 13: Effective Resistance of Line Model vs. Line Voltage

5.2 Hardware

The OTA based transmission line model was constructed in hardware using the LM13700 dual OTA and tested. Tests similar to the PSpice simulations were conducted. The effective resistance of the circuit was calculated from measurements while varying the bias voltage. The hardware exhibits similar controllable resistance as the software simulations with only slight deviation from simulation results as shown in Figure 14. Analysis shows the offset voltage present in hardware is slightly higher, and subsequently closer to the data sheet specifications, than the PSpice model.

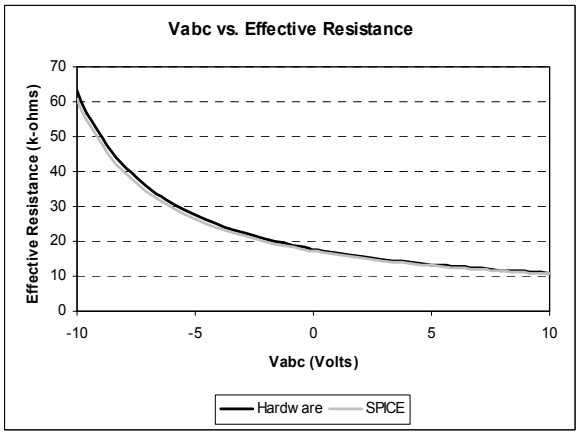

Figure 14: Hardware and Spice Effective Resistance vs. Bias Voltage

Multiple hardware tests were conducted to analyze the saturation effects of the circuit. The circuit was configured with a constant bias current and subjected to a varying line voltage. Figure 15 shows results of these tests for eight different resistance configurations. The slope of plots is indicative of the effective resistance and is constant for a limited line voltage range before saturation sets in similar to the simulations results. Figure 16 shows line current and the linear characteristic of this line current plotted against line voltage. The response is very linear and deviates only slightly in this range. This linearity is exhibited in the effective resistance of the circuit.

The effective resistance is plotted against line voltage in Figure 17. With the line voltage range between ± 2.5 volts the variance of the effective resistance was less than 1%. This is an accurate range for operation of this model. The line model becomes less accurate, saturation effects become more severe, as the line current magnitude approaches the bias current magnitude. The linear range for this model, defined by < 1% variance of effective resistance, is quantified by the following relationship:

$$i_{line} \leq 0.3 \cdot i_{abc} \qquad (11)$$

Within device limitations the line voltage can be any magnitude as long as the relationship in (11) is maintained. This is advantageous as the linear operating voltage range has been significantly increased from a basic open loop OTA with the use of feedback. This will allow easy measurement of the bus voltages in an emulation network.

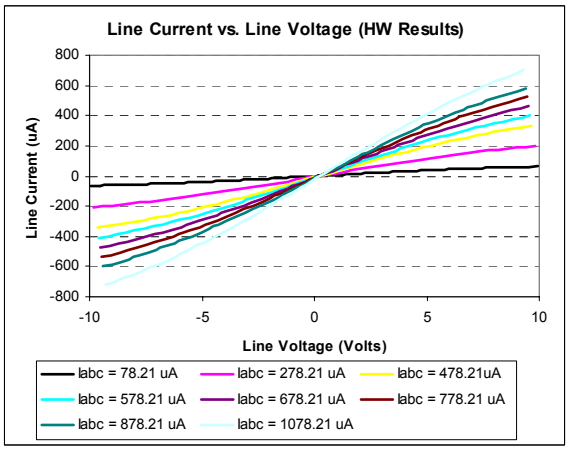

Figure 15: HW Line Current vs. Line Voltage for Various Bias Currents

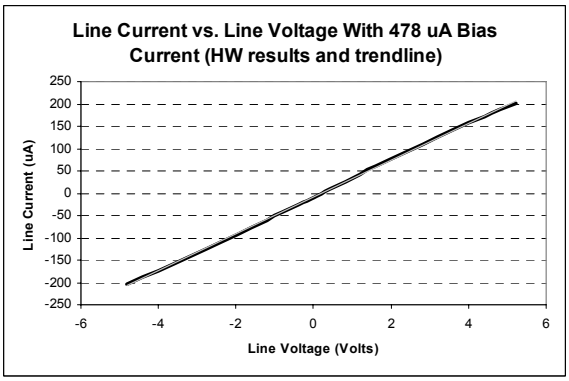

Figure 16: Line Current Linearity

The results from both simulation and hardware were very similar and verify the operation, control and linear

operating conditions of the proposed OTA based transmission line model. A three bus prototype was constructed and tested based on these results.

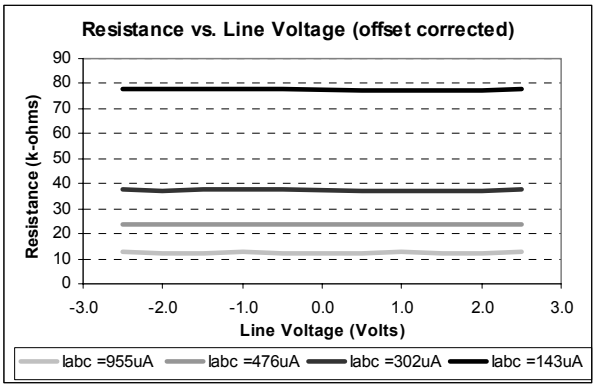

Figure 17: HW Resistance vs. Line Voltage

5.3 Three Bus Prototype

A network module prototype of a three bus power system was built based on the proposed transmission line model. This design was incorporated on a single circuit board containing the transmission line components of the four networks as shown in Figure 1. It is suitable for both lossy and lossless models shown in Figure 2 and Figure 3 respectively. The main purpose of this prototype was to validate the transmission line models application in the previously proposed DC emulation power flow technique [1]. The configuration of the power system is shown in Figure 18.

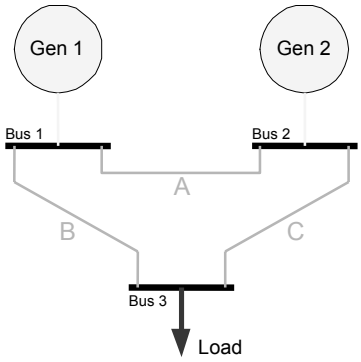

Figure 18: Three Bus Power System Topology

The power system consists of one load, two generators and three transmission lines (A, B, C). Four independent networks containing three OTA based variable resistors were used in this emulation. The combination of these networks constitutes the complete transmission line model. The circuit board developed contains only the line models with terminals to attach generator and load models. The complete circuit board is shown in Figure 19. The lines (A, B, C) are highlighted in the picture to show the relationship to the power system along with the labeling of the four networks in relation to Fig 1. The input terminals for Generators, loads, and power supply are also shown. For simplistic operation with fewer power supplies all the bias currents are driven by the +15 volt supply. Configuration of the lines was accomplished by the respective values of R_{abc}. In addition, there are jumpers on the board that connect the transmission lines to the buses. Lines can be removed for contingency analysis or the network can be reconfigured with these jumpers. In addition, this design is scalable and subsequently larger power systems can be emulated with interconnection of multiple boards.

The network module was configured for power flow emulation. DC voltage sources were used as generators (values were obtained from a computed steady-state power flow solution) and the load was an OTA based constant current source. This is shown in Figure 20. While this setup requires the prior knowledge of the generator bus voltages, the appropriate voltage on the load bus corresponding to the correct load currents is sufficient to verify the functionality of the network module. The results were compared to results from PowerWorld software package [11].

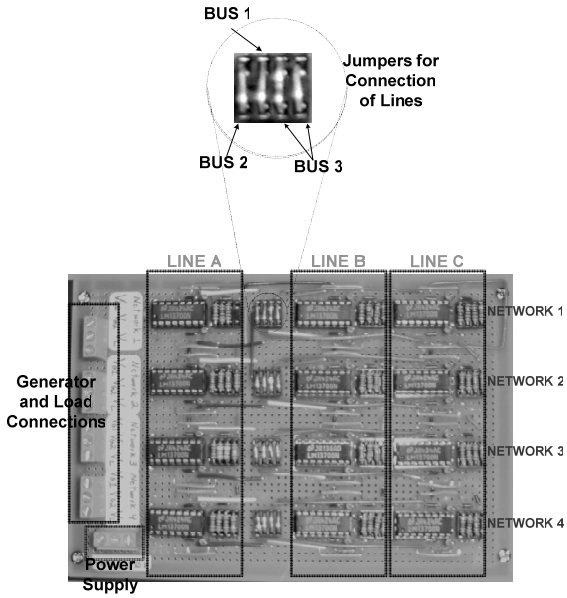

Figure 19: Three Bus Prototype Board

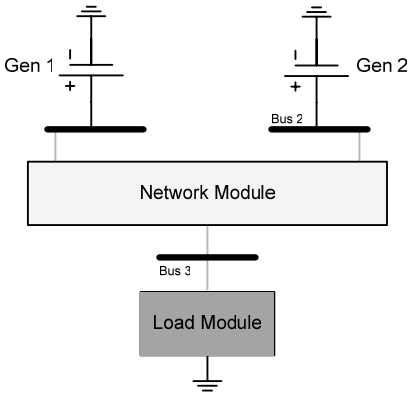

Figure 20: Emulation Circuit Setup

The network module was configured per the lossless system in PowerWorld shown in Figure 21. Table 1 shows the results, load bus voltage in per unit, from

both the hardware (offset corrected) and the software computation.

	Load Bus Voltage	
	Rectangular	Polar
PowerWorld	$0.78 + i0.25$	$0.816 \angle 17.48^\circ$
HW Emulation	$0.78 + i0.24$	$0.817 \angle 17.35^\circ$

Table 1: PowerWorld and HW Emulation Results

The results in this case are very accurate. From multiple runs and different load configurations the voltage magnitude error between PowerWorld and HW was approximately 1.5% and the phase angle error was about 5%. The errors are caused mostly by deviations from OTA to OTA and resistor tolerances.

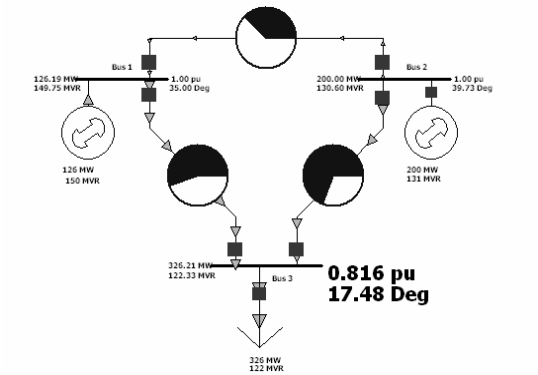

Figure 21: PowerWorld Power Flow Solution

6 DISCUSSION

The transmission line model presented is sufficient for lossy and lossless line models for use in the DC emulation static power flow technique mentioned. The overall model consists of multiple OTA based variable resistor circuits. The shortcomings of the hardware prototype, such as linear range, accuracy and device offsets, are mostly due to the current OTA technology. This can be overcome with further development of better performing OTAs, which have been shown in prior research, in a similar manner in which traditional op-amps have been developed. This problem can also be tackled through a custom VLSI design.

7 CONCLUSION

An accurate, low-cost and remotely reconfigurable OTA based analog transmission line model has been developed. Simulation and hardware results verified the design, clearly defined linear operating ranges and examined the deficiencies of current off the shelf OTAs while pointing out methods of compensation. A three bus power system was constructed based on the proposed model and the resultant power flow results compared favorably to those from commercially available software. This expands on the work presented in [1, 2, 4] by the introduction of a hardware based line model with fast, remote reconfigurability suitable for the presented power flow emulation scheme.

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