Analog Behavioral Models and the Design of Analog Emulation Engines for Power System Computation

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Abstract – This paper addresses the use of Analog Behavioral Models (ABMs) in an efficient strategy for designing analog emulation engines for large scale power system computation. Through discussion of historical development of analog computation in power system analysis and its present resurgence, we present the need for, and application of ABMs for model verification and validation prior to full structural design and implementation. Results of PSpice simulations of these emulation circuits are also presented and compared with industrial grade numerical simulations for validation.

Keywords: Analog Behavioral Models (ABMs), Analog emulation, PSpice, Power system computation, Simulation

1 INTRODUCTION

This paper attempts to address an efficient strategy for designing analog emulation engines for large scale power system computation through the use of Analog Behavioral Models (ABMs) of PSpice [1]. Analog emulation of large power systems as compared to the currently in use numerical/digital approaches will have a clear advantage in computation time, which is faster and independent of network size and topology [2]. It must be mentioned that the ABMs approach may be a first step towards feasible realization of an analog emulation engine built of real analog components and devices. It does not serve as a substitute for neither the components nor the building blocks.

Emulation can be described as an act of a physical system imitating a real system. Emulation in this paper therefore, is the representation of physical characteristics of a real life object (power system) using an electric circuit equivalent. The representation relationship could be mathematical, scaled, or both. The circuit equivalent representation has within it, the model of a real system, as well as a method of its solution. The speed of computation is as quick as the response of the circuit itself; which could be real-time, faster or slower than real-time depending on the parameters setting. The solution is continuous in time and amplitude.

Simulation on the other hand is an attempt to predict/replicate aspects of the behavior of a real system by creating an approximate (mathematical) model of it. This is done by computer modeling; by writing a special-purpose computer program. The program is composed of equations that describe the functional relationships within the real system. When the program is run, the resulting mathematical dynamics form an analog of the behavior of the real system, with the results presented in the form of data.

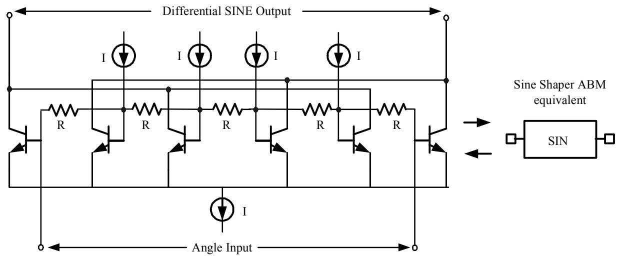

Figure 1: Analog and ABM Sine Shaper

The need to emulate/simulate large and complex mixed-signal systems has prompted the development of high-level circuit representation for analog components; ABMs serve this purpose. In this paper, ABMs are used to make flexible descriptions of electronic components or complex building block in terms of transfer function or lookup tables. In order words, a mathematical relationship is used to model a circuit segment, so one will not need to design the segment component by component. Figure 1 shows a sine shaper which is a device that outputs sine value of its input signal. The left side of Figure 1 is a modified Gilbert sine shaper [3] built component by component using analog devices, and the right side of Figure 1 is an ABM sine shaper [1]. The only similarity between the two is that they both take the same input signal and produce the same output. The interior of a behavioral model however, is different in that it is implemented in terms of algebraic or differential equations rather than physical analog components. In order words, in a behavioral model, the focus is on the input/output relationship of the block. The fundamental advantage of the behavioral modeling technique in top-down designs is that the simulation can provide fast prediction of system performance. The approach helps to select proper architectures for circuit implementation and analyze tradeoffs at the early design stages. The transistor-level simulation (bottom-up design) comparatively can be very tedious and cumbersome especially for mixed-signal chips containing a large number of analog components. Under such circumstances, behavioral models enable designers to

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verify the complex system efficiently and result in fast system evaluation prior to embarking on full structural design and implementation. In this paper, ABMs are used as building blocks to develop software simulation of an analog emulation engine that computes the states and behaviors of a power system. Analysis is limited to load flow only.

This paper is presented in the following manner. In the next section, a brief historical background of power system computation using analog, the currently-in-use digital/numeric counterpart, and the resurgence of analog emulators will be presented. Section 3 will present methodology of power system core computation using ABMs. Discussions on tested sample cases, PSpice simulation results and results from currently in-use industrial-grade numerical simulators for the purpose of comparison and validation, will be given in Section 4. Finally, the paper is summarized in Section 5.

2 BACKGROUND

Simulation and/or emulation are indispensable when dealing with large-scale power systems. They make it possible to do essential assessment in power system dispatch, operation, security and stability. Different simulation/emulation tools today are built for different applications like transient stability analysis, fault analysis, power flow studies, operational planning, etc. The history of power system techniques of simulation or emulation dates back to the start of last century. Krause et al [4] give a good review of the subject as do McLaren et al [5]. The building of these simulators/emulators has been based either on analog, digital or combination of analog and digital implementations as shown in Figure 2. Analog emulation consists of building a scaled-down model of a real power system. This may include using analog devices that represent equations characterizing distinct relationships within the power system. Digital simulation consists of developing digital computer programs that solve network mathematical equations through numerical methods. These simulators/emulators have their advantages and disadvantages or short comings in their mode of operation, functionality, efficiency and accuracy.

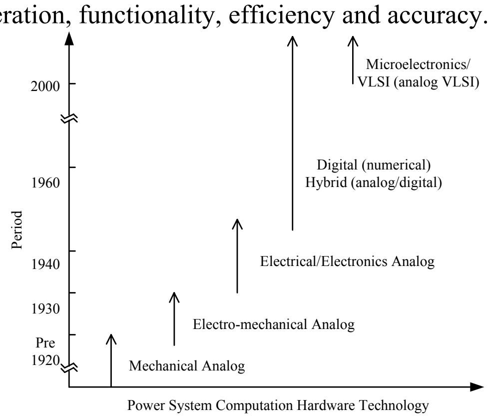

Figure 2: Time Line of Hardware Technology

Technology has naturally been an important factor in the development of power system computation tools. The first emulators were analog. Analog computing devices, instruments, and machines have been widely in use since ancient times. Analog computation has gone through transitions such as mechanical, electromechanical, electrical, and electronic developments as depicted in Figure 2. Electrical analog emulation techniques were predominant from 1920 to 1950. The earlier analog computers were special or fixed purpose, and then general-purpose. The special-purpose analog emulator technique forms the basis of both the Power System Transient Network Analyzer (TNA) and the High Voltage Direct Current (HVDC) analog emulator [6]. Their implementations allow for real-time or faster than real-time emulation however, there were serious limitations on the reconfiguration and size of the system that can be emulated. This is because of their special purpose built nature and the technology of devices used. Other disadvantages of this implementation include, but are not limited to complexity, accuracy and cost of maintenance of the emulator. General-purpose electronic analog computers on the other hand could be used for a variety of applications. By altering the arrangements of interconnections between the computing elements, they could be set up, or programmed to solve many different problems [7]. Its disadvantages which include size and accuracy were influenced more by the technology of the time. Figure 3 depicts structural comparison between old and proposed technologies of analog emulation engine for power system computation.

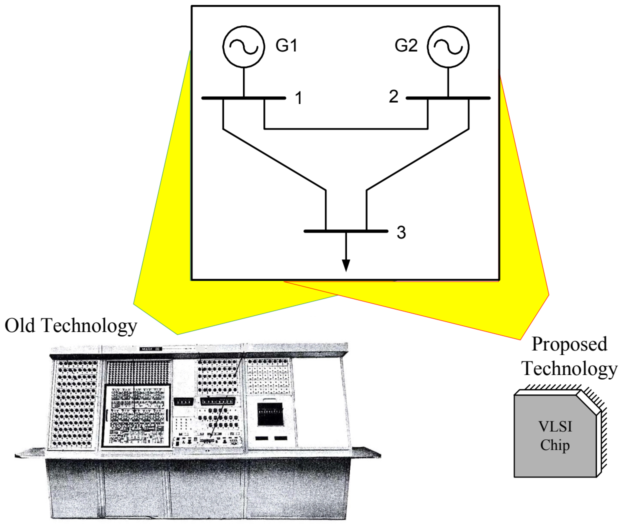

Figure 3: Comparison of Old and Proposed Technology

In the late fifties began the application of digital computers to solving power system problems. Due to higher precision, flexibility and ease of simulating larger systems, digital simulators began to replace analog emulators. However, one of the most significant disadvantages of software based simulators relates to the speed at which they operate. They are limited by the "clock rate,"- the number of steps that can be executed in a second. For example, present clock rates though fast, do not allow for real-time computation of large-scale power systems.

Consequently, digital simulations are severely limited in time-critical applications like on-line monitoring and control.

Following the advent of the digital computer emerged the hybrid computer. Hybrid computers combined the fast computation features of analog with the logic and accuracy of digital computers. This technique greatly enhanced the efficiency of once-pure-analog emulators such as power system transient network analyzer (TNA) [8]. However, the size of hybrid TNA emulator depends largely on the work required of it. That is, the larger the real power system network to be emulated, the larger the emulator.

There are extensive and ever continuing efforts to improve and expand the capabilities and applications of digital (numerical) simulators; to achieve the goal of real-time. Some of the efforts include: (i) fast decoupled power flows; (ii) sparse matrix computation techniques to reduce the elements to be computed as zero elements take time and spaces; (iii) parallel processing using multiple high speed CPU's; (iv) LU decomposition to help avoid inversion of large matrices that proves cumbersome and time consuming [9]. But the clock rate still limits the effects of the enhancements. More so, Newton-Raphson method which is the most widely used method for solving simultaneous nonlinear algebraic equations in power systems is sequential. It uses a successive approximation procedure based on an initial estimate of the unknown and the use of Taylor's series expansion.

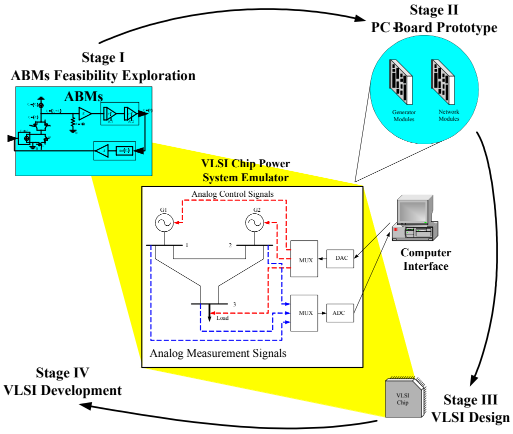

Figure 4: Developmental Stages of an Analog Emulator

There has been recent advancement in the areas of microelectronics and VLSI technology that allows hundreds of thousands to millions of active components (most often transistors) to be placed on a chip on the order of 100 mm^2 in area and 0.5 mm thick [10]. Analog technology is now a viable candidate for implementing power system emulator. Other examples of application of analog implementation are in domains such as neural modeling, visual processing, and associative memories [10]. The goal of making real-time computation a reality may well require a rebirth of technology that many consider obsolete in this era of digital computer — analog computers (emulators). Therefore the focus of this paper is the feasibility exploration of design of analog emulation engine for power systems computation using ABMs. Figure 4 gives a pictorial summary of developmental stages to the goal - implementation of analog emulator on a VLSI chip. The methodology of implementation of power system core computation is discussed next.

3 METHODOLOGY OF CORE COMPUTATIONS USING ABMs

Analog Behavioral Models (ABMs) of PSpice are used to build a scaled-down model of a real power system. This may include using ABMs that represent equations characterizing distinct relationships within the power system. The approach is only for the purpose of design feasibility studies. The main advantage is that it gives a clearer picture of the end goal, design layouts and intricacies of circuit connections.

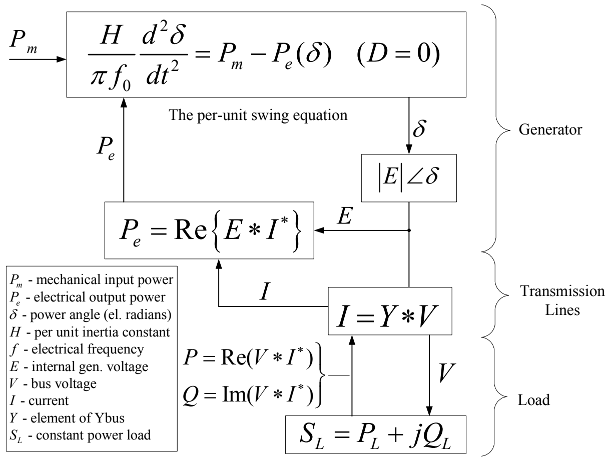

Figure 5: Block Diagram of Core Computation Methodology of an Analog Emulator

Power system core computation methodology implemented in the design of analog emulation goes through three major steps. These steps are illustrated in Figure 5. The assumptions made and detail processes are discussed in [11] and [2], respectively.

Step 1: Calculating complex voltage out of generator

The generator block solves the swing equation (dynamic) with resulting power angle, δ. The power angle combines with desired voltage magnitude to give a complex voltage out of a generator.

Step II: Calculating currents in the network

The nodal and generator induced voltages interact with transmission line impedance and load (if not lumped with line impedance) to produce complex current flowing in any branch. Using admittance for simplicity and expressing in rectangular form, current is computed as in Figure 5. As depicted in Figure 6, it will require four separate networks in order to emulate complex current flowing on any branch. The approach of dc-resistive network as proposed by Fried et al [11] is used. Transformation of the transmission line complex impedance to its resistive value for real and imaginary part is through its complex conjugate as shown in equation 1.

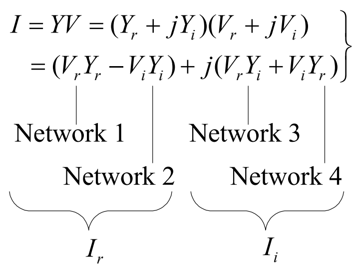

Figure 6: Complex Current Computation Methodology

$$
\left.\begin{aligned}
Y &= \frac{1}{Z} = \frac{1}{R + jX} = \frac{R - jX}{R^2 + X^2} \\
Y_{\mathrm{Re}} &= \frac{R}{R^2 + X^2} = Y_r \\
Y_{\mathrm{Im}} &= (-)\frac{X}{R^2 + X^2} = Y_i
\end{aligned}\right\} \qquad (1)
$$

Combining equation 1 with Figure 6, we can show the implementation of complex current computation as described in Figure 7.

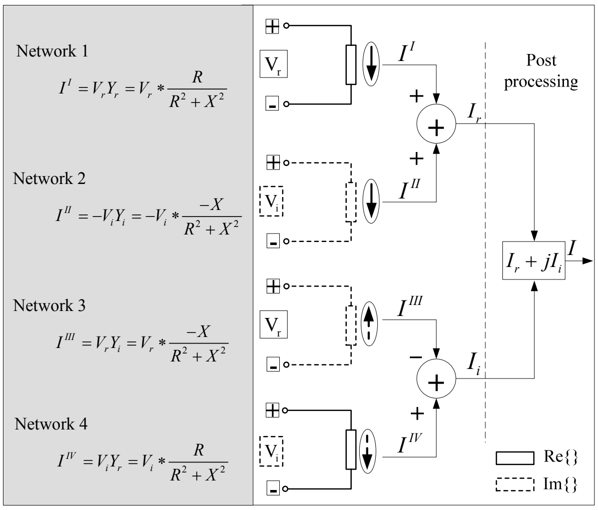

Figure 7: Complex Current Computation Implementation

This means that the real part of complex current flowing in any branch is given by the sum of component currents in networks 1 and 2, and the imaginary part as the difference between component currents in networks 4 and 3, as described in equation 2.

$$
\left.\begin{aligned}
I &= I_r + jI_i \\
I_r &= I^I + I^{II} \\
I_i &= I^{IV} - I^{III}
\end{aligned}\right\} \qquad (2)
$$

where subscripts r and i represent real and imaginary part, respectively. I, II, III, IV represent the four DC networks.

Step III: Computation of generator real power and swing equation update

The real power out of each generator in the system is calculated as the real part of the product of generator terminal voltage and complex conjugate of the generator current:

$$P_{e_i} = \mathrm{Re}\left\{E_{g_i} * I_{g_i}\right\} = \mathrm{Re}\left\{E_{g_i}\right\} * \mathrm{Re}\left\{I_{g_i}\right\} + \mathrm{Im}\left\{E_{g_i}\right\} * \mathrm{Im}\left\{I_{g_i}\right\} \quad (3)$$

The swing equation describes the dynamics of a generator. Its input is a mechanical power from prime mover and which is assumed constant. The output of a generator is an electrical power, which changes in accordance with the state of the network. The swing equation is a second order differential equation and its solution is the power angle of the generator. The power angle combines with generator internal voltage to constantly update the generator terminal voltage and hence the generator current. Figure 8 describes the continuous cycle of power system core computation.

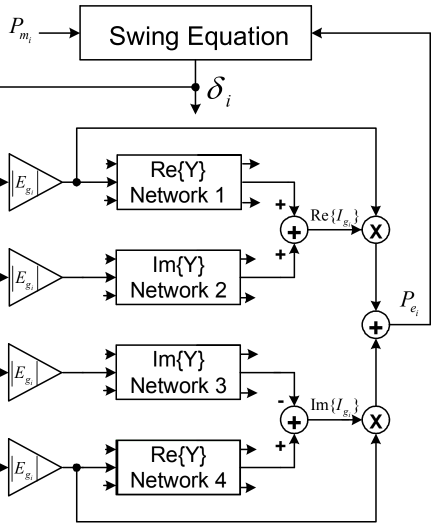

Figure 8: Generator Real Power Computation Methodology

Figure 9 describes the dc-network equivalent of a real power system bus and conditions for its implementation. Analyzing a sample power system and considering an arbitrary bus k with its complex voltage values, we have 4 networks with 4 buses: k^I, k^{II}, k^{III} and k^{IV} as equivalents. For feasible bus voltages, the following conditions must be satisfied:

$$
\left.\begin{aligned}
V_{k^I} &= V_{k^{III}} = V_{k_r} \\
V_{k^{II}} &= V_{k^{IV}} = V_{k_i}
\end{aligned}\right\} \qquad (3)
$$

It is then and only then that the current computation methodology described in section 3 will yield accurate and feasible values. The feasible bus voltages condition is realizable with a constant PQ-load model [2].

Among other attributes of an analog emulator that contribute greatly to its versatility are the scale factors. Scale factors are constants that relate the values of the variables on the emulator to the values of the variables in the real system under study. The choice of proper scale factors is an important consideration in obtaining satisfactory results [2].

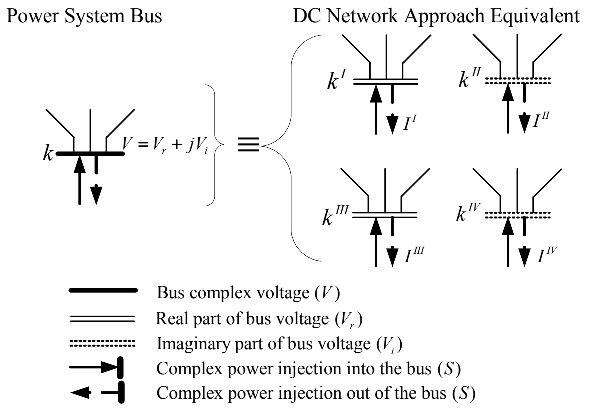

Figure 9: Computationally Feasible Bus Voltage

4 CASE STUDIES AND RESULTS

Cases studied which include 3-bus, 6-bus and 14-bus lossy and lossless power systems were implemented using ABMs of PSpice. ABMs substitute real analog circuit implementation of the mathematical equations and scaled relationship that describe the states of the power system cases and emulate their behaviors. Power flow test were conducted on each of the cases. Similar cases were tested on industrial grade numerical simulation software, PowerWorld v9.1 [12] and Power System Simulation for Engineering (PSS/E) v.28.1 [13], for benchmarking. For the validation process, the following parameters were measured and/or calculated and compared with the benchmarks.

i. δ_{j1} – Voltage angle difference between generator buses j and 1 (j = 2, 3, …);
ii. Load bus complex voltage;
iii. Current magnitude flowing in each branch.

Simulation results obtained from the analog emulation engines implemented on ABMs of PSpice and that of the benchmarks are presented in Tables 1 through 4. It must be mentioned that the following limitations were encountered during measurements (or computations) of the benchmarks parameters:

- The PowerWorld Simulator [12] computes only magnitude of a branch current;
- The PSSE [13] provides a bus voltage angle to one decimal place, and only the magnitude of a branch current.

From the Tables, we conclude that the emulation results compares favorably. This confirms the validity of the methodology as well as the technique of implementation.

$$\left.\begin{matrix} P \\ Q \end{matrix}\right\} \rightarrow I \text{ (1 pu : 1 A)}$$

$$\delta \rightarrow V \text{ (1 radian : 1 volt)}$$

$$I \rightarrow V \text{ (1 A : 1 volt)}$$

Figure 10: Variable Representation in Analog Emulator

Simulation outputs of analog emulator were measured in rectangular form and/or radians. Conversions to polar representation and/or degree were made for easy comparisons with the benchmarks. Also, for convenience and efficient analog emulation implementation, certain power system variables and parameters were represented by other circuit variables. Figure 10 summarizes variable representations used in this work. Since conversion ratio used between current-voltage or power-current is 1:1, obtained values remain representative in quantity.

Table 1: Summary Results for 3-bus Power System (lossless system)

	PowerWorld	PSS/E	Analog Emulator
Relative Power Angle (δ_{21}) in degree	0.94°	0.9°	0.94°
Load Bus (V3) Voltage (Vpu)	$0.988\angle{-3.17}°$	$0.988\angle{-3.2}°$	$0.9880\angle{-3.17}°$
Current in Branch 2_1 (I, A)	343.18	343	343.2
Current in Branch 1_3 (I, A)	784.49	784.5	784.5
Current in Branch 2_3 (I, A)	503.87	503.9	503.9

Table 2: Summary Results for 3-bus Power System (lossy system)

	PowerWorld	PSS/E	Analog Emulator
Relative Power Angle (δ_{21}) in degree	0.65°	0.6°	0.65°
Load Bus (V3) Voltage (Vpu)	$0.9675\angle{-1.03}°$	$0.968\angle{-1}°$	$0.9675\angle{-1.03}°$
Current in Branch 2_1 (I,A)	334.26	334	334.6
Current in Branch 1_3 (I,A)	691.39	691	691.6
Current in Branch 2_3 (I,A)	654.24	654	654.2

Table 3: Summary Results for 6-Bus Power System (Lossy System)

	PowerWorld	PSS/E	Analog Emulator
Relative Power Angle (δ_{21}) in degree	-2.10°	-2.10°	-2.10°
Relative Power Angle (δ_{31}) in degree	-2.71°	-2.7°	-2.71°
Load Bus (V4) Voltage (Vpu)	$0.974\angle{-7.35}°$	$0.974\angle{-7.3}°$	$0.974\angle{-7.35}°$
Load Bus (V5) Voltage (Vpu)	$0.988\angle{-4.69}°$	$0.988\angle{-4.7}°$	$0.988\angle{-4.69}°$
Load Bus (V6) Voltage (Vpu)	$0.983\angle{-6.36}°$	$0.983\angle{-6.4}°$	$0.9829\angle{-6.36}°$
Current in Branch 1_2 (I, A)	344.86	345	344.86
Current in Branch 1_5 (I, A)	758.72	759	758.72
Current in Branch 2_5 (I, A)	388.84	389	388.84
Current in Branch 2_6 (I, A)	515.05	515	515.04
Current in Branch 3_6 (I, A)	376.53	377	376.54

Table 4: Summary Results for 14-Bus Power System (Lossless)

	PowerWorld	PSS/E	Analog Emulator
Relative Power Angle (δ_{21}) in degree	-1.08°	-1.1°	-1.08°
Relative Power Angle (δ_{31}) in degree	-0.75°	-0.8°	-0.75°
Relative Power Angle (δ_{61}) in degree	-8.09°	-8.1°	-8.09°
Relative Power Angle (δ_{81}) in degree	-7.30°	-7.3°	-7.30°
Load Bus (V4) Voltage (Vpu)	$0.989\angle -5.51°$	$0.989\angle -5.5°$	$0.989\angle -5.51°$
Load Bus (V5) Voltage (Vpu)	$0.991\angle -4.75°$	$0.991\angle -4.8°$	$0.991\angle -4.75°$
Load Bus (V7) Voltage (Vpu)	$0.984\angle -9.22°$	$0.984\angle -9.2°$	$0.984\angle -9.22°$
Load Bus (V9) Voltage (Vpu)	$0.979\angle -11.15°$	$0.979\angle -11.2°$	$0.979\angle -11.15°$
Load Bus (V10) Voltage (Vpu)	$0.980\angle -11.68°$	$0.980\angle -11.7°$	$0.980\angle -11.68°$
Load Bus (V11) Voltage (Vpu)	$0.987\angle -10.70°$	$0.987\angle -10.7°$	$0.987\angle -10.70°$
Load Bus (V12) Voltage (Vpu)	$0.982\angle -12.42°$	$0.982\angle -12.4°$	$0.982\angle -12.42°$
Load Bus (V13) Voltage (Vpu)	$0.980\angle -12.88°$	$0.980\angle -12.9°$	$0.980\angle -12.88°$
Load Bus (V14) Voltage (Vpu)	$0.979\angle -11.20°$	$0.979\angle -11.2°$	$0.979\angle -11.20°$
Current in Branch 1_5 (I, A)	311.63	312.63	311.63
Current in Branch 2_5 (I, A)	309.85	309.85	309.85
Current in Branch 5_4 (I, A)	262.5	262.5	262.5
Current in Branch 4_9 (I, A)	151.21	151.21	151.21

5 SUMMARY

Analog Behavioral Models of PSpice simulation software is a very efficient tool. Among advantages are that it gives opportunity to test drive ideas, it aids in exploring the effects of modifications, and etc. However, it should be mentioned that ABMs and PSpice simulation tool are in no way a substitute for real analog block or analog emulation engine. These tools are free of noise, crosstalk or interference. For real analog implementation, issues like component variations, stray conductive paths, and others have to be dealt with.

Technology has naturally been an important factor in the development of power system computation tools. The implementations have gone through various stages of development. Evolution of microelectronics and VLSI technology whereby millions of active components can be placed on a chip on the order of $100\ mm^2$ in area and $0.5\ mm$ in thickness, now cause the resurgence of what was once considered old technology – analog computation. This latest technology makes analog emulation a viable candidate for quicker computation of power system states and behaviors considering its intrinsic massively parallel collective processing capability.

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