ELEN0037
Microelectronics
Tutorials

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Tutorial 7: Nyquist rate and oversampling A/D Converters

Signal to Quantization Noise Ratio (summary)

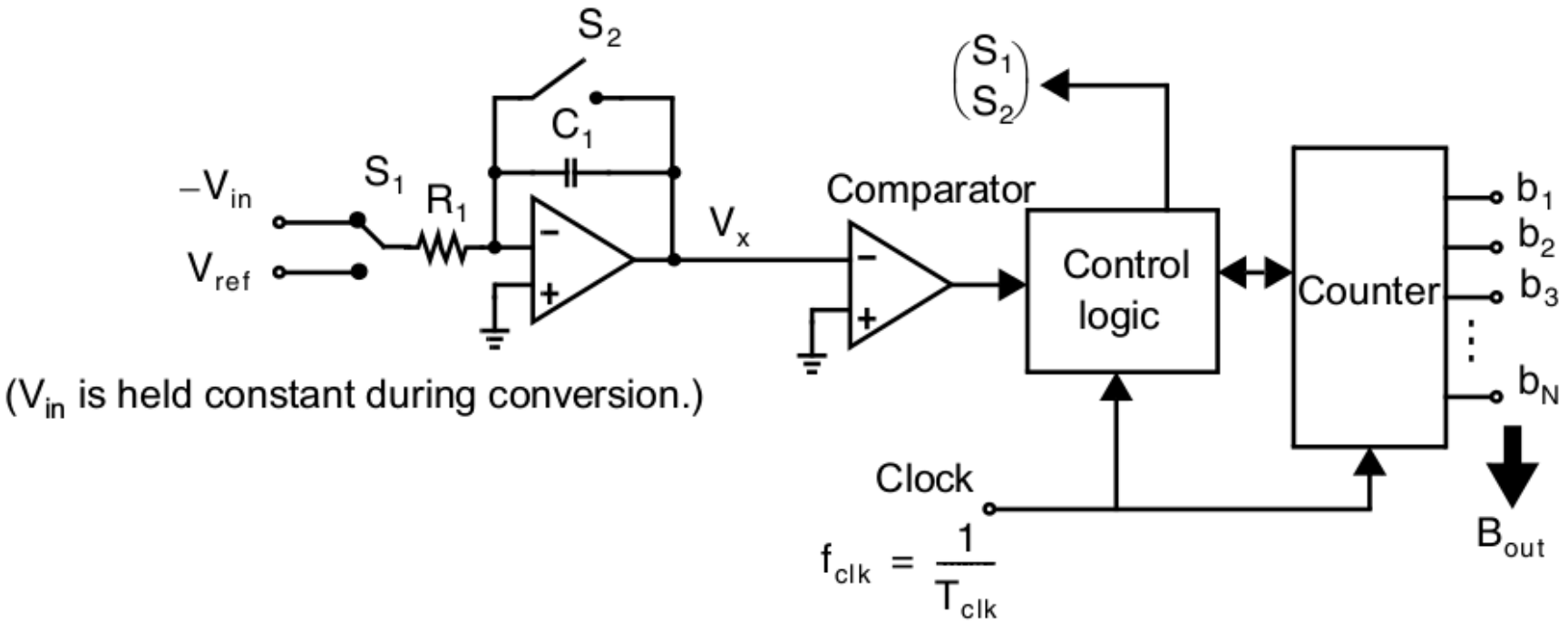
converter type	$SQNR_{max}$
Nyquist rate	$6.02N + 1.76$
Oversampling with no noise shaping	$6.02N + 1.76 + 10 \log OSR$
Oversampling with 1^{st}-order noise shaping	$6.02N + 1.76 - 5.17 + 30 \log OSR$
Oversampling with 2^{nd}-order noise shaping	$6.02N + 1.76 - 12.9 + 50 \log OSR$

$$OSR = \frac{f_s}{2f_0}$$

Note that these formulae are valid for an input sine wave (otherwise remove the $+1.76$ term), when the input signal spans the full range of the converter.

Exercise 1 (1st, P13.1/2nd, P17.1)

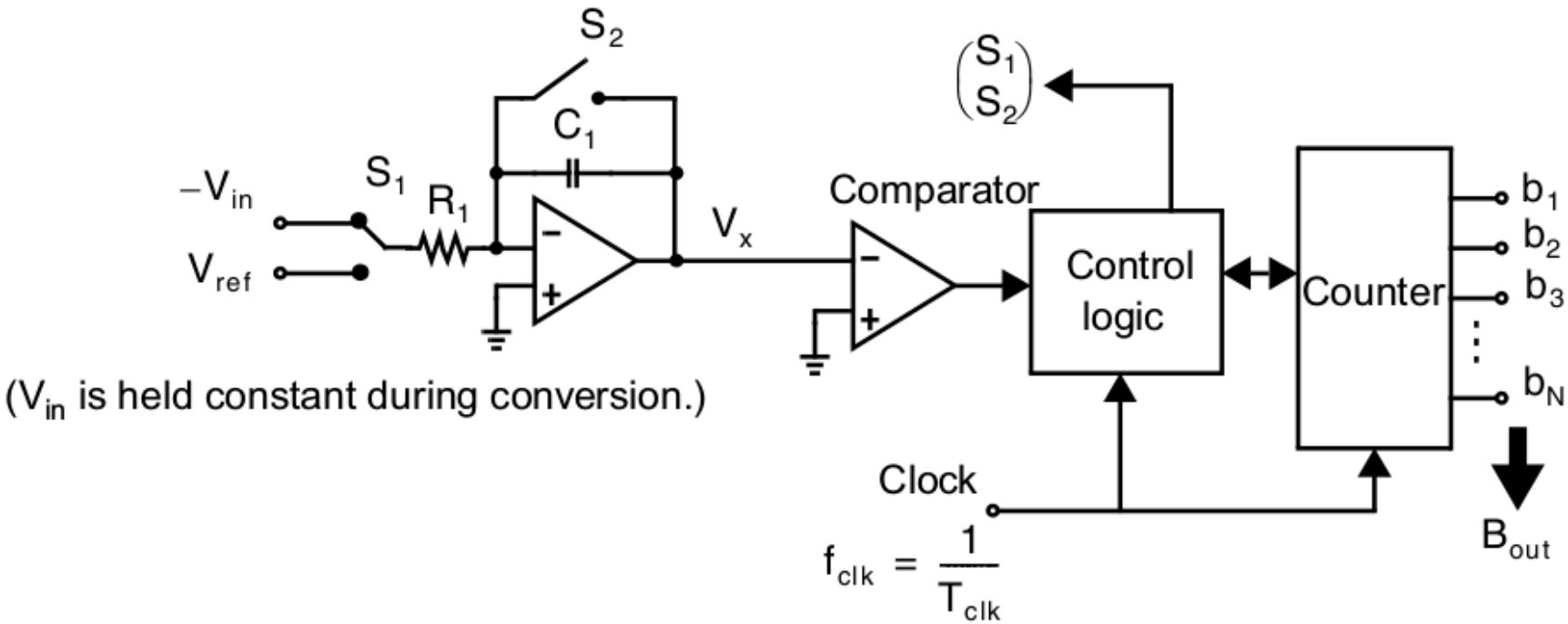
What is the worst-case conversion time for an 18-bit dual-slope integrating A/D converter when the clock frequency is 5 MHz?[1]



[1] $T_{conv,max} = \left(2.2^N + 1\right) T_{clk} = 105\,ms$

Exercise 2 (1st, P13.2/2nd, P17.2)

Consider an 18-bit dual-slope integrating A/D converter, where V_{ref} equals $10\,V$, $C_1 = 100\,pF$, and a clock frequency of $1\,MHz$ is used. What value of R_1 should be chosen such that the opamp output never exceeds $10\,V$ when $0\,V < V_{in} < 10\,V$?[2]



[2] $R_1 > 2.62\,G\Omega$

Exercise 3 (1st, P13.5,6/2nd, P17.5,6)

What input-signal frequencies are completely attenuated by a 16-bit dual-slope integrating A/D converter, having a clock frequency of $1\,MHz$?[3] For this same converter, what is the attenuation of an input signal at $60\,Hz$?[4] Repeat the same, when $f_s = 100\,kHz$.[5]

[3] all frequencies multiple of $1/T_1 = 1/2^N T_{clk} = 15.26\,Hz$

[4] $A_{f=60\,Hz} = 1.98\,10^{-2} = -34\,dB$

[5] all frequencies multiple of $1.53\,Hz$, $A_{f=60\,Hz} = 5.09\,10^{-3} = -46\,dB$

Exercise 4 (1st, P14.1)

Assuming oversampling with no noise shaping, find the approximate sampling rate required in order to obtain a maximum SQNR of $80\,dB$ on a signal with a $1\,kHz$ bandwidth using a 1-bit quantizer.[6] Repeat the same problem, assuming a first-order modulator is used.[7] Repeat the same problem, assuming a second-order modulator is used.[8]

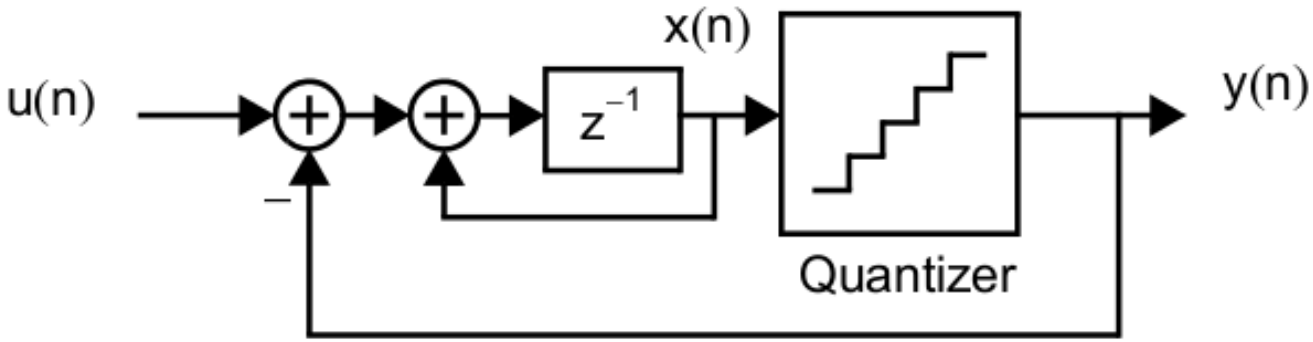
[6] $OSR = 16672472$, $f_s = 33.35\,GHz$

[7] $OSR = 380$, $f_s = 760\,kHz$

[8] $OSR = 50.4$, $f_s = 100.8\,kHz$

Exercise 5 (1st, P14.2,3,4/2nd, P18.4,5,6)

Find the output and state values of a 1^{st}-order $\Sigma\Delta$ modulator using a 1-bit quantizer (± 1 output levels, $threshold = 0$), when a dc input $u(n) = 0.4$ is applied, and assuming the initial state $x(0) = 0.1$.[9] At what frequency would a tone appear (relative to f_s)?[10]



The state equations of the first-order $\Sigma\Delta$ modulator are given by:

$$\begin{aligned} y(n) &= Q(x(n)) \\ e(n) &= y(n) - x(n) \\ x(n+1) &= x(n) + u(n) - y(n) \end{aligned}$$

[9] see next slide

[10] $f_s/10$

Exercise 5 (continued)

The output and state values are given in the following table. Also, compute $e_{rms} = {}^{\Delta}/_{\sqrt{12}}$, $\sqrt{(E\{e^2(n)\})}$, and $E\{y(n)\}$.[11]

n	$u(n)$	$x(n)$	$y(n)$	$e(n)$	$x(n+1)$
0	0.4	0.1	1	0.9	−0.5
1	0.4	−0.5	−1	−0.5	0.9
2	0.4	0.9	1	0.1	0.3
3	0.4	0.3	1	0.7	−0.3
4	0.4	−0.3	−1	−0.7	1.1
5	0.4	1.1	1	−0.1	0.5
⋮	⋮	⋮	⋮	⋮	⋮
10	0.4	0.1	1	0.9	−0.5

[11] $e_{rms} = 0.577\,V$, $\sqrt{(E\{e^2(n)\})} = 0.611\,V$, $E\{y(n)\} = 0.4\,V$

Exercise 5 (continued)

Repeat the same problem, with a dc input $u(n) = 1.1$, and the same initial state, to see if the internal state $x(n)$ of the modulator saturates.[12]

n	$u(n)$	$x(n)$	$y(n)$	$e(n)$	$x(n+1)$
0	1.1	0.1	1	0.9	0.2
1	1.1	0.2	1	0.8	0.3
2	1.1	0.3	1	0.7	0.4
⋮	⋮	⋮	⋮	⋮	⋮

[12] $x(n)$ increases by 0.1 at each clock cycle, until saturation occurs

Exercise 5 (continued)

Repeat the same problem, with the following input sequence: $\{10, -10, 10, -10, 10, \ldots\}$, and the same initial state, to see if the internal state $x(n)$ of the modulator saturates.

n	$u(n)$	$x(n)$	$y(n)$	$e(n)$	$x(n+1)$
0	10	0.1	1	0.9	9.1
1	-10	9.1	1	-8.1	-1.9
2	10	-1.9	-1	0.9	9.1
3	-10	9.1	1	-8.1	-1.9
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$

Exercise 6 (1st, P14.5,6/2nd, P18.3,7)

Given that an 8-bit A/D converter has a SQNR of $50\,dB$ but is linear to 12 bits, what is the sampling rate required to achieve 12 bits of accuracy using straight oversampling on a signal bandwidth of $1\,MHz$?[13] What becomes the sampling rate if this 8-bit A/D converter is placed inside a first-order $\Sigma\Delta$ modulator?[14] What becomes the sampling rate if the 8-bit A/D converter is placed inside a second-order $\Sigma\Delta$ modulator?[15]

[13] $OSR = 256$, $f_s = 512\,MHz$
[14] $OSR = 9.44$, $f_s = 18.88\,MHz$
[15] $OSR = 5.49$, $f_s = 10.98\,MHz$