ELEN0037
Microelectronics
Tutorials

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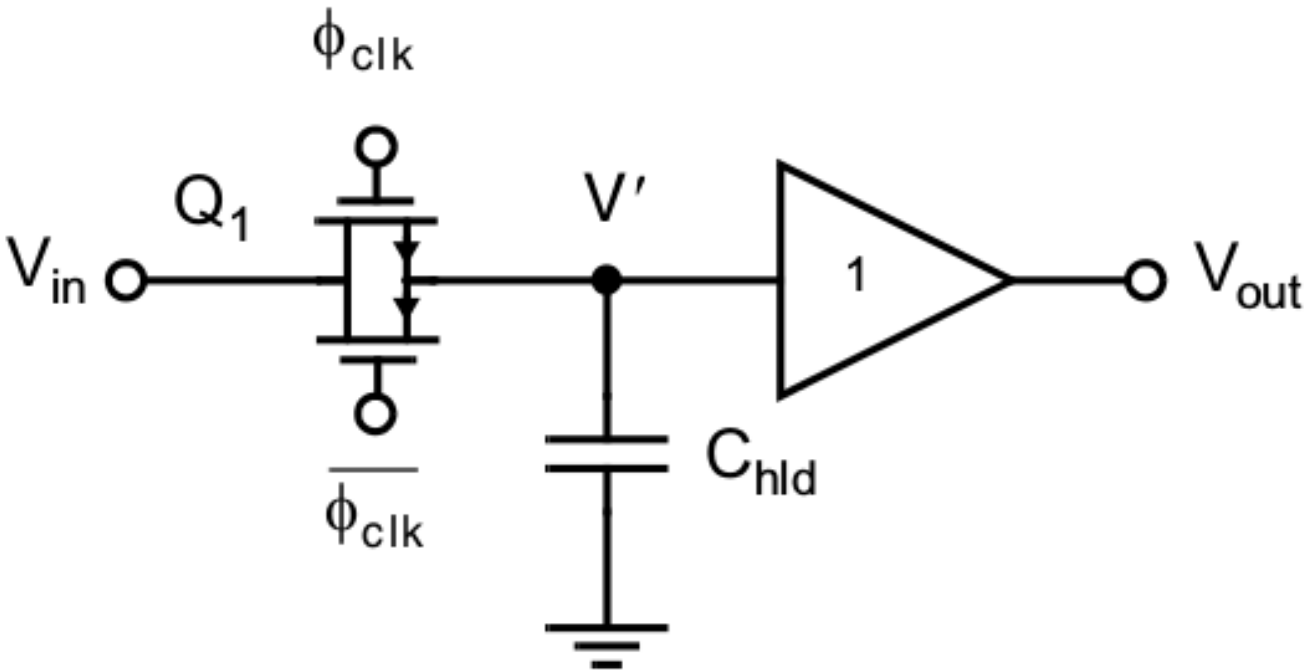
Tutorial 3: Sample and Holds, Switched-Capacitor circuits

Exercise 1 (1st, P8.2/2nd, P11.4)

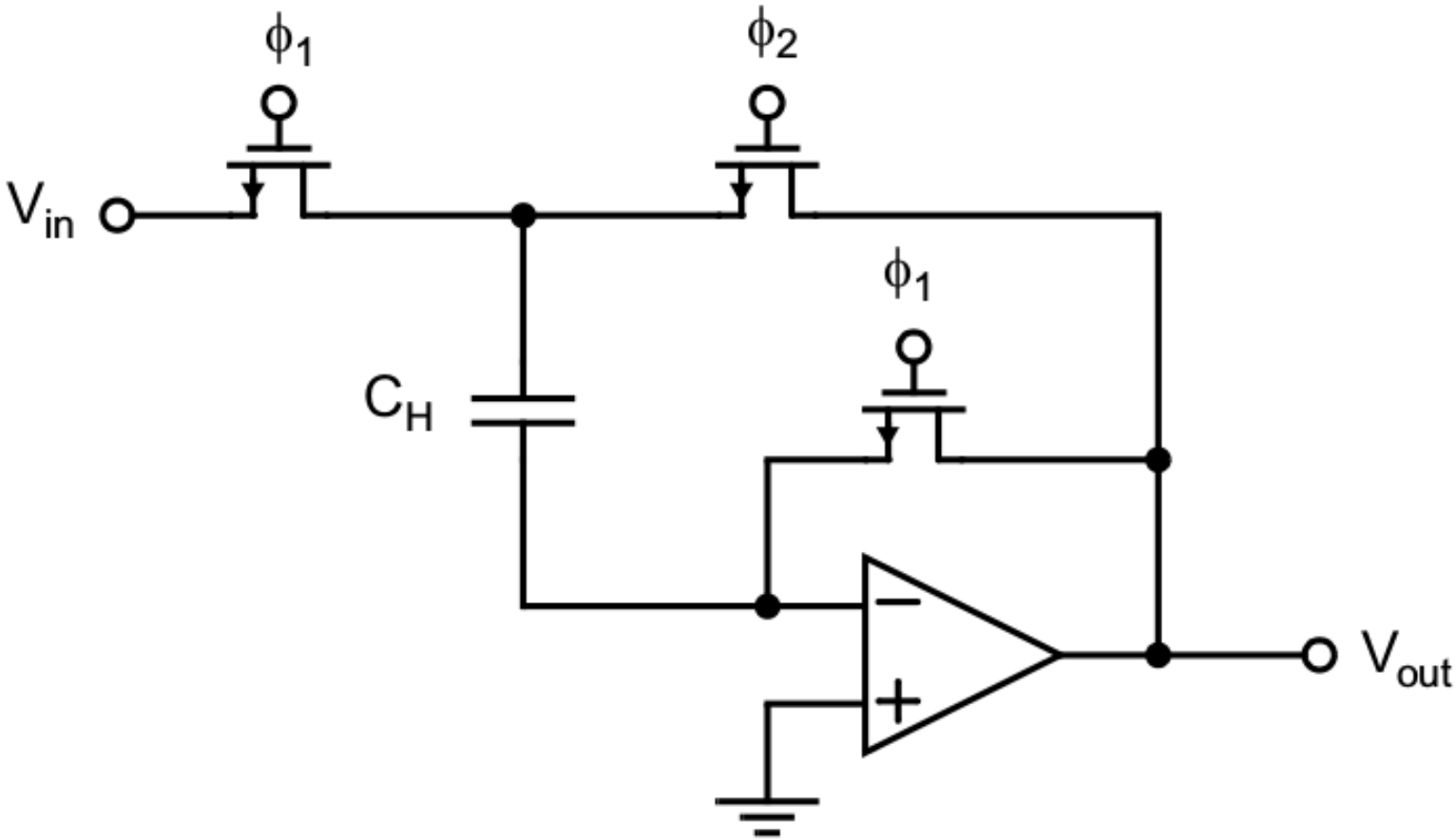
In the following S/H circuit, assume V_{in} is a $20\,MHz$ sinusoid with a $2\,V_{pp}$ amplitude. Also assume that ϕ_{clk} is a $100\,MHz$ square wave having a peak amplitude of $\pm 2.5\,V$ with rise and fall times of $1.5\,ns$. What is the maximum time difference between the turn-off times of the n-channel and p-channel transistors?[1] Ignore the body effect ($V_{tn} = 0.8\,V$, $V_{tp} = -0.9\,V$).



[1] $|\Delta\phi|_{max} = 2.1\,V$, $\Delta t_{max} = 0.63\,ns$

Exercise 2 (1st, P8.6/2nd, P11.8)

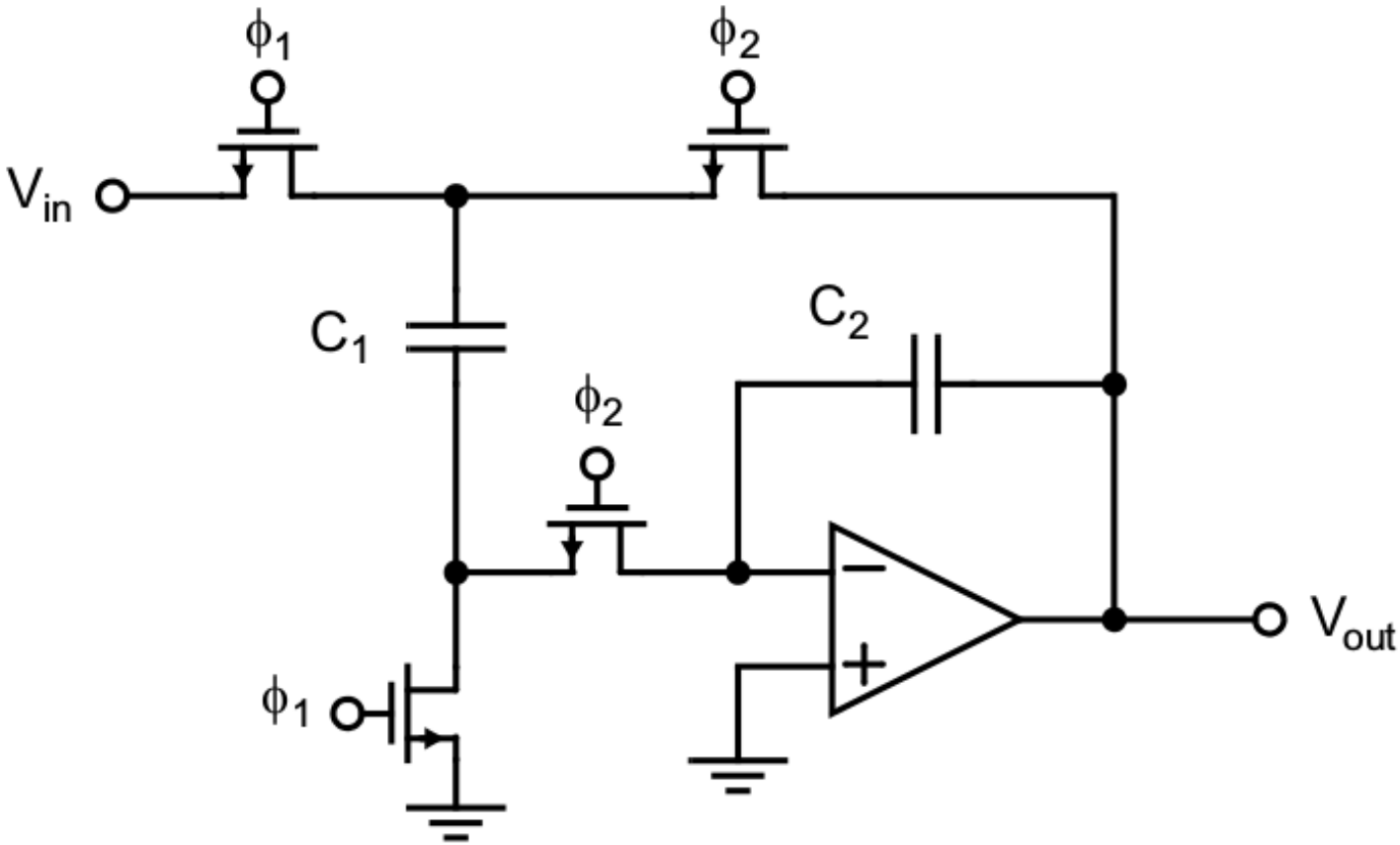
Assume the opamp of the following S/H circuit has a finite gain of A, and offset voltage V_{offset}. Derive the output voltage in terms of V_{in}, A, and V_{offset} during hold mode (i.e., when ϕ_2 is high).[2]



[2] $V_{out} = \frac{A}{A+1} V_{in} + \frac{A}{(A+1)^2} V_{offset}$

Exercise 3 (1st, P8.7/2nd, P11.9)

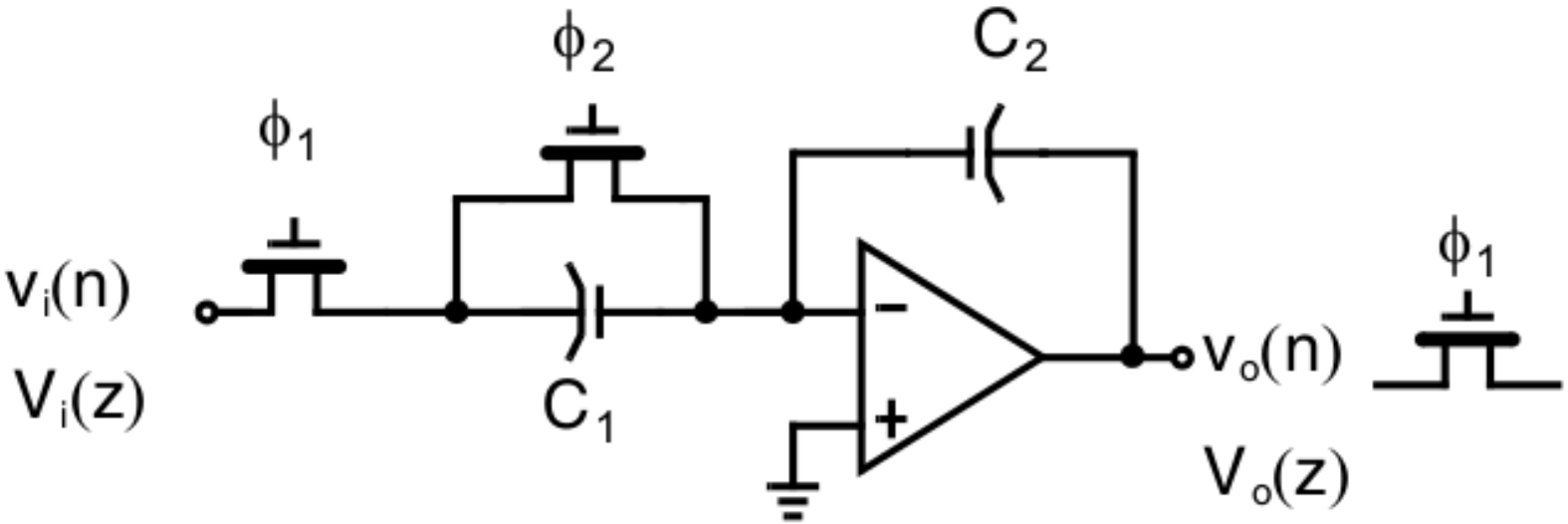
Derive the frequency-domain transfer function of the following S/H circuit (use $z = e^{j\omega T}$), and find the cut-off frequency f_{-3dB}. Make the assumption that $e^{j\omega T} \cong 1 + j\omega T$ for $\omega T \ll 1$.[3]



[3] $H(z) = \frac{z^{-1}}{1+C_2/C_1(1-z^{-1})}$, $f_{-3dB} = \frac{1}{2\pi}\frac{C_1}{C_2}f_s$

Exercise 4 (1st, P10.2/2nd, P14.4)

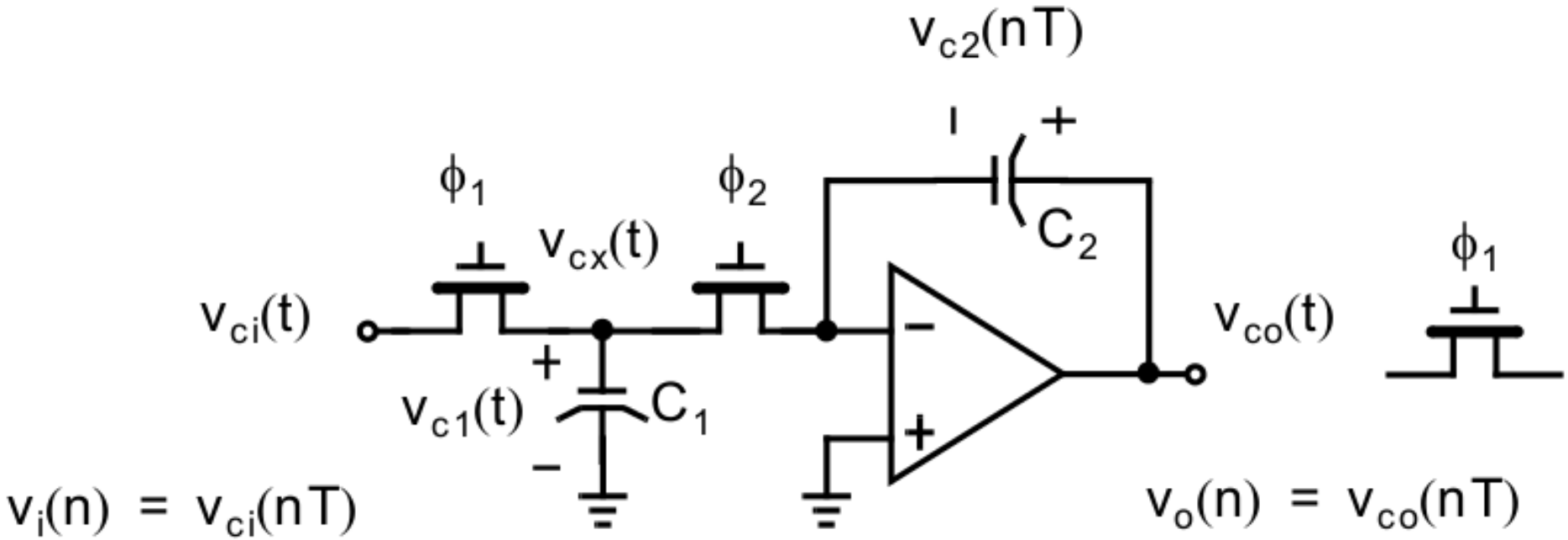
Ignoring the effect of parasitic capacitances, find the discrete-time transfer function of the following switched-capacitor circuit.[4]



[4] $H(z) = -(C_1/C_2)\frac{1}{1-z^{-1}}$ (delay-free inverting integrator)

Exercise 5 (1st, P10.4/2nd, P14.6)

Compute the transfer function of the following discrete-time integrator, when the opamp has a finite gain of A.[5] Also show that this transfer function has a DC gain of $-A$ and a pole that is located slightly to the left of 1.



[5] $H(z) = -(C_1/C_2)(A/A+1)\frac{z^{-1}}{1-(1-C_1/C_2(A+1))z^{-1}}$, $z_p = 1 - \frac{C_1}{C_2}\frac{1}{A+1} \lesssim 1$